IN THE CLAIMS:

1. An apparatus for controlling a data transfer between a data processor and a data unit, comprising:

a first control unit that controls the data transfer between the data processor and the data unit, the first control unit including a first memory device; and

a second control unit that controls the data transfer between the data processor and the data unit, the second control unit including:

a second memory device; and

a memory controller that enables the second control unit access to the first and second memory devices.

2. The apparatus of claim 1,

the memory controller including:

a first logic unit that obtains access to the first memory device; and

a second logic unit that enables a data transfer to the first and second memory devices concurrently.

3. The apparatus of claim 1,

the memory controller including:

a third logic unit that receives an indication of a memory failure to the first memory device and which disables the memory controller from accessing the first memory device.

4. The apparatus of claim 1,

the memory controller including:

a fourth logic unit that receives an indication of a memory failure to the second memory device and which disables the second control unit from controlling the data transfer between the data processor and the data unit.

5. The apparatus of claim 1, comprising:

a first communications link that transfers data between the data processor and the first and second control units; and

a second communications link that transfers data between the data unit and the first and second control units.

6. The apparatus of claim 5,

wherein the first communications link is a Fibre Channel; and

wherein the second communications link is a SCSI channel.

7. In a method for controlling a transfer of data between a data processor and a data unit, said method comprising the steps of:

providing a plurality of control units, each control unit having a capability to control the transfer of data between the data processor and the data unit, each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device;

selecting one of the control units as a master control unit to control the transfer of data between the data processor and the data unit;

designating a second one of the control units as a slave control unit;

utilizing the memory device in the master control unit for the data transfer between the data processor and the data unit; and

synchronizing the memory device in the master control unit with the memory device in the slave control unit.

8. The method of claim 7,

the synchronizing step further comprising the steps of:

generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device;

transferring a subset of the generated signal paths to the signal paths associated with the slave memory device; and

allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

9. The method of claim 8,

the generating step further comprising the step of:

generating, in the master control unit, values for the signal paths associated with the slave memory device that enable access to the slave memory device.

10. The method of claim 8, further comprising the steps of:

associating an address and control signal path with each memory device that enables access to the corresponding memory device;

the generating step further comprising the step of:

producing values for the address and control signal paths associated with the master memory device; and

the transferring step further comprising the step of:

transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the slave memory device.

11. The method of claim 10, further comprising the steps of:

associating with the master memory device a first control signal that controls access to the slave memory device;

associating with each memory device a second control signal that controls access to the corresponding memory device;

the generating step further comprising the step of:

producing values for the first control signal and the second control signal associated with the master memory device;

the transferring step further comprising the step of:

transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device.

12. The method of claim 10, further comprising the steps of:

associating with each control unit a data signal path;

the transferring step further comprising the step of:

receiving data values for the data signal path associated with the master memory device; and

transmitting the received data values to the data signal path associated with the slave memory device.

13. The method of claim 8, further comprising the steps of:

associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path; and

enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths.

14. The method of 13, further comprising the step of:

disabling the control mechanism associated with a memory device to inhibit a transfer and receipt of signal path values.

15. The method of claim 7, further comprising the steps of:

suspending the master control unit from controlling the data transfer between the data processor and the data unit;

enabling the slave control unit to control the transfer of data between the data processor and the data unit; and

utilizing the memory device in the slave control unit for the data transfer between the data processor and the data unit.

16. The method of claim 15,

the suspending step further comprising the step of:

determining that the master control unit has experienced an operational failure.

17. The method of claim 16,

the determining step further comprising the step of:

receiving an indication that the memory device in the master control unit has failed.

18. The method of claim 7, further comprising the steps of:

disabling the master control unit from accessing the slave memory device; and

suspending operation of the slave control unit.

19. The method of claim 17,

the disabling step further comprising the step of:

determining that the slave control unit has experienced an operational failure.

20. An apparatus for controlling a data transfer between a data processor and a data unit, comprising:

a first control having a capability to control the data transfer between the data processor and the data unit, comprising:

a first memory controller generating a first address signal, a first control signal, and a first switch control signal;

a first memory device coupled to the first memory controller, the first memory device receives the first address signal, the first control signal, and a first data signal to perform a memory access; and

a first switch control unit that allows the first control unit to receive data values for the first address signal, the first control signal, and the first data signal, the first switch control unit coupled to the first switch control signal, the first address signal, the first control signal, and the first data signal;

a second control unit that controls the data transfer between the data processor and the data unit, comprising:

a second memory controller generating a second address signal, a second control signal, and a second switch control signal;

a second memory device coupled to the second memory controller, the second memory device receives the second address signal, the second control signal, and a second data signal, to perform a memory access; and

a second signal switch control unit that allows the second control unit to transmit data values from the second address signal to the first address signal, from the second control signal to the first control signal, and from the second data signal to the first data signal, the second signal switch control unit coupled to the second switch control signal, the second address signal, the second control signal, and the second data signal.

21. The apparatus of claim 20,

the first switch control unit further including:

a first address switch coupled to the first address signal and the first switch control signal, the first address switch enables receipt of data values for the first address signal;

the second switch control unit further including:

a second address switch coupled to the second address signal, the second switch control signal, and the first address switch, the second address switch enables transmission of data values from the second address signal to the first address signal;

wherein the first switch control signal controls the first address switch to receive data values; and

wherein the second switch control signal controls the second address switch to transmit data values.

22. The apparatus of claim 20,

the first switch control unit further including:

a first data switch coupled to the first data signal and the first switch control signal, the first data switch enables receipt of data values for the first data signal;

the second switch control unit further including:

a second data switch coupled to the first data switch, a second data signal, and the second bus control signal, the second data switch enables transmission of data values from the second data signal to the first data signal;

wherein the first switch control signal controls the first data switch to receive data values; and

wherein the second switch control signal controls the second data switch to transmit data values.

23. The apparatus of claim 20,

the first switch control unit further including:

a first control switch coupled to the first control signal and the first switch control signal, the first control switch enables receipt of data values for the first control signal;

the second switch control unit further including:

a second control switch coupled to the second control signal, the second switch control signal, and the first control switch, the second control switch enables transmission of data values from the second control signal to the first control signal;

wherein the first switch control signal controls the first control switch to receive data values; and

wherein the second switch control signal controls the second control switch to transmit data values.

24. The apparatus of claim 21,

the first control unit further comprising:

a first address buffer that receives the first address signal and transmits the first address signal to the first memory device;

the second control unit further comprising:

a second address buffer that receives the second address signal and transmits the second address signal to the second memory device.

25. The apparatus of claim 22,

the first control unit further comprising:

a first data buffer coupled to a first data signal, the first data buffer transmits the first data signal to the first memory device; and

the second control unit further comprising:

a second data buffer coupled to a second data signal, the second data buffer transmits the second data signal to the second memory device.

26. The apparatus of claim 23,

the first control unit further comprising:

a first control buffer coupled to the first control signal and the first switch control signal, the first control buffer transmits the first control signal to the first memory device;

the second control unit further comprising:

a second control buffer coupled to the second control signal and the second bus control signal, the second control buffer transmits the second control signal to the second memory device.

27. The apparatus of claim 24,

wherein the first address switch is positioned between the first memory controller and the first address buffer; and

wherein the second address switch is positioned between the second memory controller and the second address buffer.

28. The apparatus of claim 26,

wherein the first control switch is positioned between the first memory controller and the first control buffer; and

wherein the second control switch is positioned between the second memory controller and the second control buffer.

29. The apparatus of claim 22,

wherein the first data switch is positioned between the first data buffer and the first memory device; and

wherein the second data switch is positioned between the second data buffer and the second memory device.

30. The apparatus of claim 25,

the first control unit further comprising:

a first bus coupled to the first memory controller and the first data buffer; and

wherein the first data buffer receives data values for the first data signal from the first bus;

the second control unit further comprising:

a second bus coupled to the second memory controller and the second data buffer; and

wherein the second data buffer receives data values for the second data signal from the second bus.

31. The apparatus of claim 20, further comprising:

a first communication link coupled to the data processor and the first and second control units, the first communications link providing a data transfer between the data processor and the first and second control units; and

a second communication link coupled to the data unit and the first and second control units, the second communications link providing a data transfer between the data processor and the first and second control units.

32. The apparatus of claim 31,

wherein the first communications link is a Fibre Channel; and

wherein the second communications link is a SCSI Channel.

33. The apparatus of claim 20,

the second memory controller including a first logic unit that controls access to the first and second memory devices; and

the first memory controller including a first logic unit that requests access to the first memory device from the second memory controller.

34. The apparatus of claim 20,

the first memory controller including a second logic unit that controls operation of the first memory controller, the second logic unit receiving a first fail signal indicating a memory failure to the first memory device, the second logic unit terminating operation of the first memory controller in response to the local fail signal; and

the second memory controller including a second logic unit that controls operation of the second memory controller, the second logic unit receiving the first fail signal from the first memory controller, the second logic unit terminating access to the first memory device.

35. The apparatus of claim 34,

the second logic unit in the first memory controller receiving a reset signal and initializing operation of the first memory controller; and

the second logic unit in the second memory controller receiving the reset signal and initializing operation of the second memory controller.

36. The apparatus of claim 20,

the second memory controller including a second logic unit that controls operation of the second memory controller, the second logic unit receiving a second fail signal indicating a failure to the second memory device, the second logic unit terminating operation of the second memory controller; and

the first memory controller including a second logic unit that controls operation of the first memory controller, the second logic unit receiving the second fail signal, the second logic unit resuming control of the data transfer between the data processor and the data unit.